CY62256V

32K x 8 Static RAM

Features

- **Low voltage range:**
  - **CY62256V (2.7V–3.6V)**
  - **CY62256V25 (2.3V–2.7V)**
- **Low active power and standby power**
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

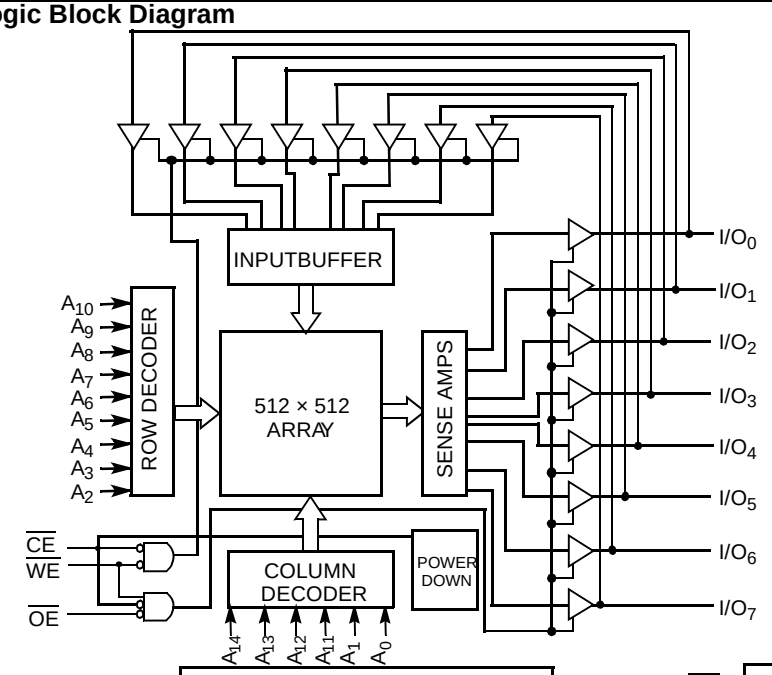
Functional Description

The CY62256V family is composed of two high-performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62256V family is available in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

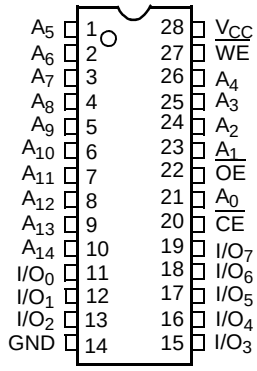
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram

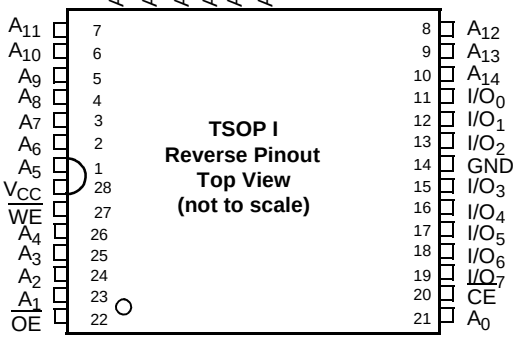


Pin Configurations

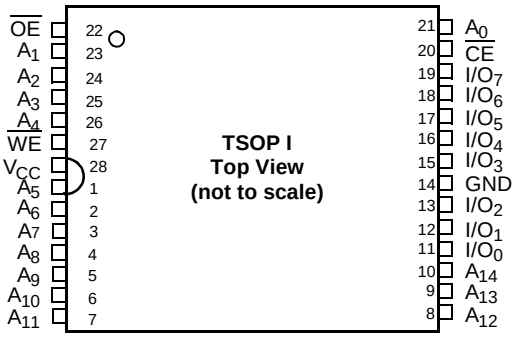
SOIC
Top View



TSOP I
Reverse Pinout
Top View
(not to scale)



TSOP I
Top View
(not to scale)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1]..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.3V to 3.6V
Industrial	–40°C to +85°C	2.3V to 3.6V

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation			
					Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
	Min.	Typ.[2]	Max.		Typ.[2]	Max.	Typ.[2]	Max.
CY62256V	2.7	3.0	3.6	70	11	30	0.1	5
CY62256V25	2.3	2.5	2.7	100	9	15	0.1	4

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62256V-70			Unit
				Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	Vcc= 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	Vcc= 2.7V			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} +0.3V	V
V_{IL}	Input Leakage Voltage			–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{IN} ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = 3.6V, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		11	30	mA
I_{SB1}	Automatic CE Power-down Current— TTL Inputs	V_{CC} = 3.6V, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		100	300	µA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	V_{CC} = 3.6V, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		0.1	5	µA
			Ind'l			10	µA

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62256V25-100			Unit
				Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	Vcc= 2.3V	2			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	Vcc= 2.3V			0.4	V
V_{IH}	Input HIGH Voltage			1.7		Vcc + 0.3V	V
V_{IL}	Input LOW Voltage			–0.3		0.7	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{IN} ≤ V_{CC}, Output Disabled		–1		+1	µA

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C, and t_{AA} = 70 ns.

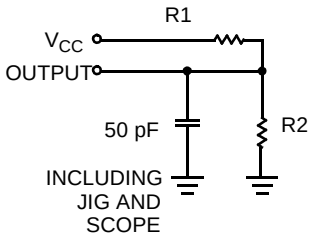
Electrical Characteristics Over the Operating Range (continued)

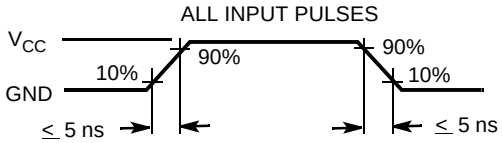
Parameter	Description	Test Conditions		CY62256V25-100 Min.	CY62256V25-100 Typ.[2]	CY62256V25-100 Max.	Unit
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = 2.7V, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		14	23	mA
I_{SB1}	Automatic CE Power-down Current— TTL Inputs	V_{CC} = 2.7V, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Com'l		75	225	µA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	V_{CC} = 2.7V, $\overline{CE} \geq V_{CC}$ – 0.3V $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V, f = 0	Com'l		0.1	4	µA
			Ind'l			8	µA

Capacitance[3]

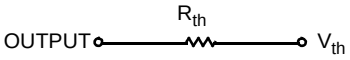
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



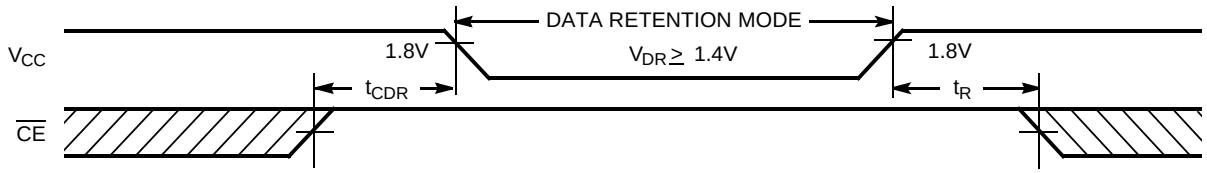
Parameter	3.3V	2.5V	Units
R1	1.100	16.60	K Ohms
R2	1.500	15.40	K Ohms
RTH	0.645	8.00	K Ohms
VTH	1.750	1.20	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[4]		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.4			V
I_{CCDR}	Data Retention Current	V_{CC} = 1.6V, $\overline{CE} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V	Com'l		0.1	3	µA
			Ind'l			6	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0			ns
t_R[3]	Operation Recovery Time			t_{RC}			ns

Notes:
3. Tested initially and after any design or process changes that may affect these parameters.
4. No input may exceed V_{CC} + 0.3V.

Data Retention Waveform



Switching Characteristics Over the Operating Range[5]

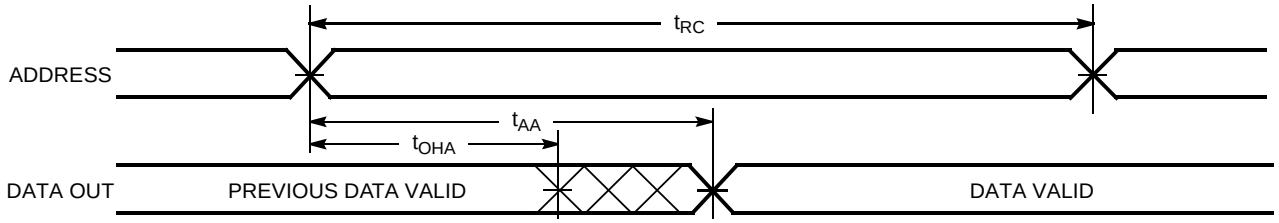
Parameter	Description	CY62256V-70		CY62256V25-100		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	70		100		ns
t_{AA}	Address to Data Valid		70		100	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70		100	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		75	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[6]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		25		50	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[6]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		25		50	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		70		100	ns
Write Cycle[8, 9]						
t_{WC}	Write Cycle Time	70		100		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		90		ns
t_{AW}	Address Set-up to Write End	60		90		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		80		ns
t_{SD}	Data Set-up to Write End	30		60		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		25		50	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	10		10		ns

Notes:

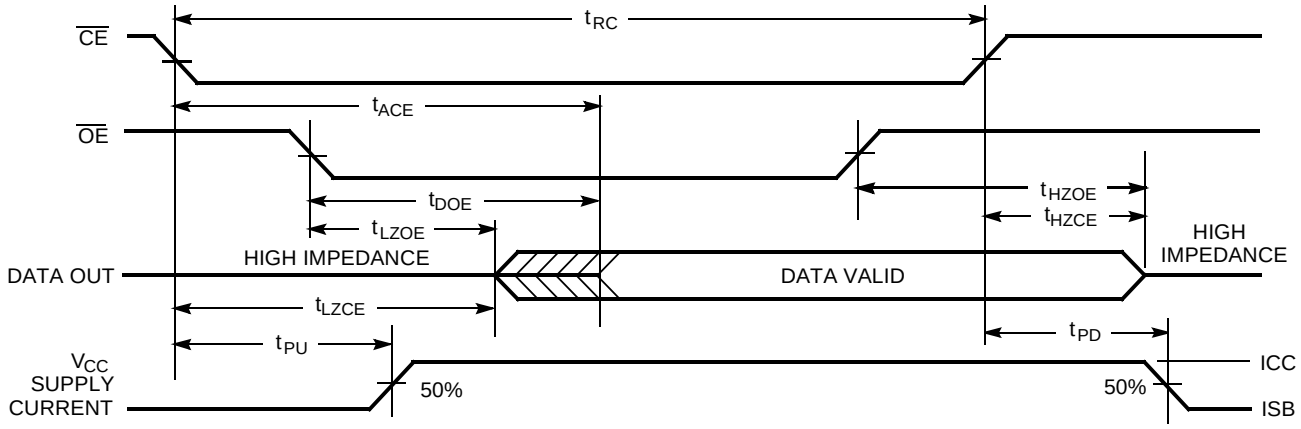
5. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC}, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

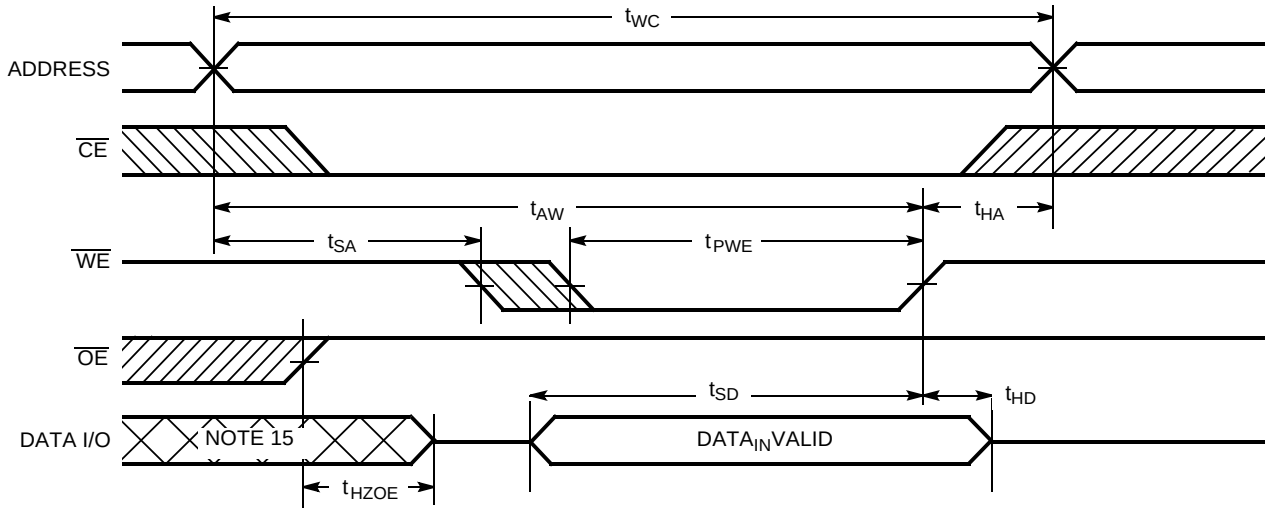
Read Cycle No. 1[10, 11]



Read Cycle No. 2 [11, 12]



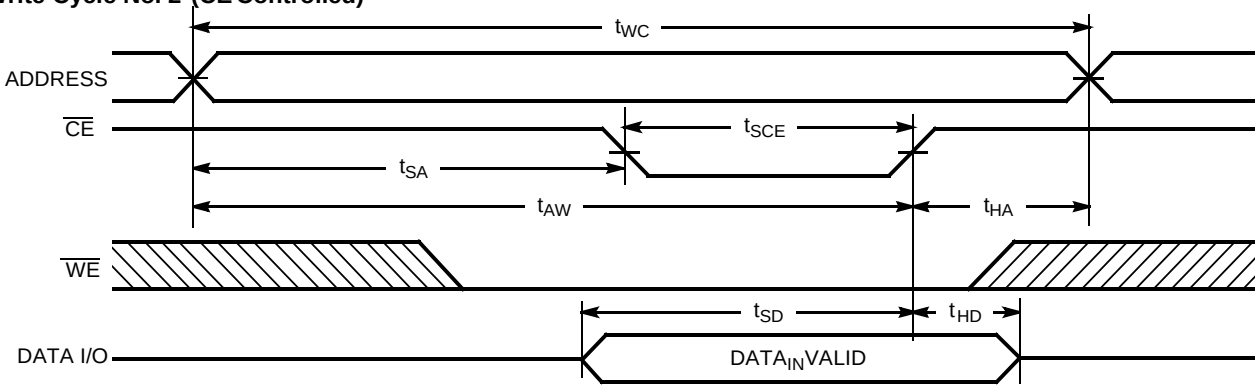
Write Cycle No. 1 (WE Controlled)[8, 13, 14]



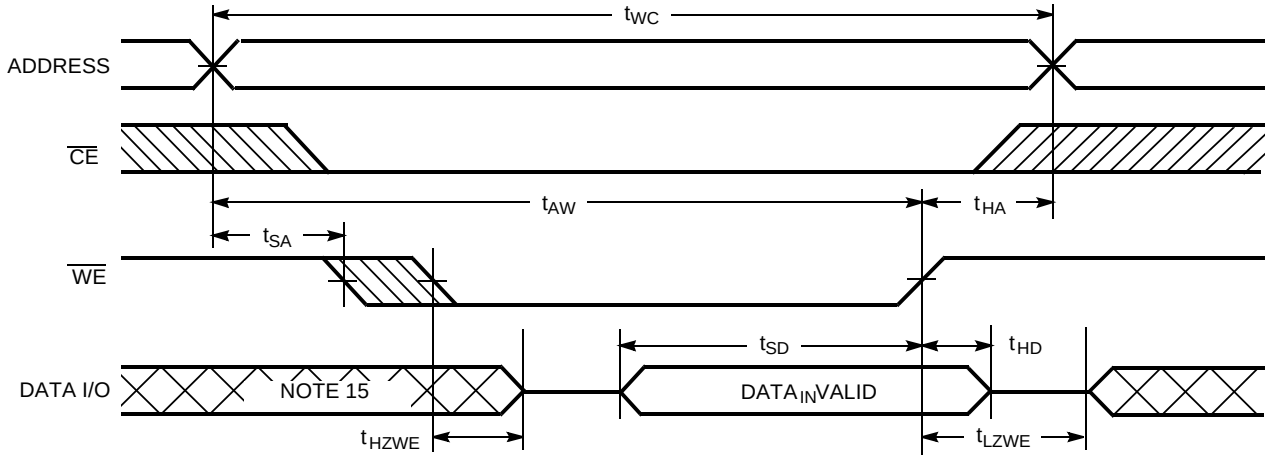
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 14]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]

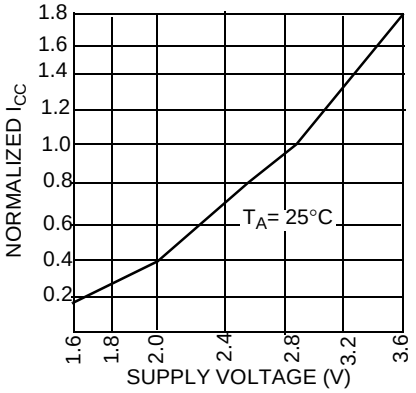


Notes:

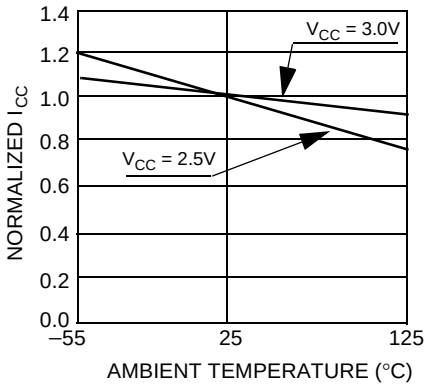
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics

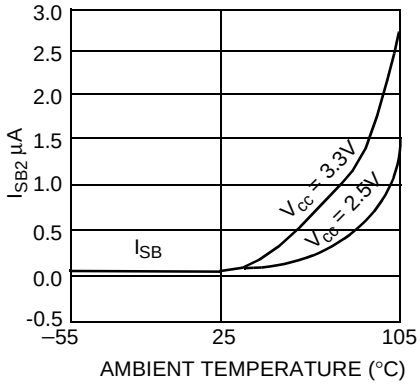
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



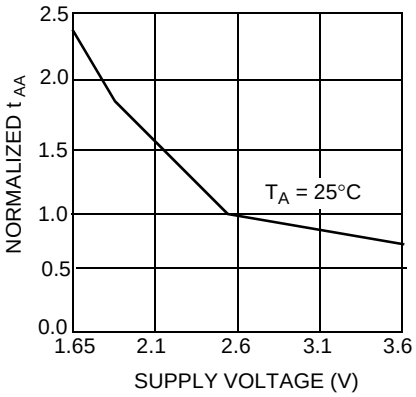
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



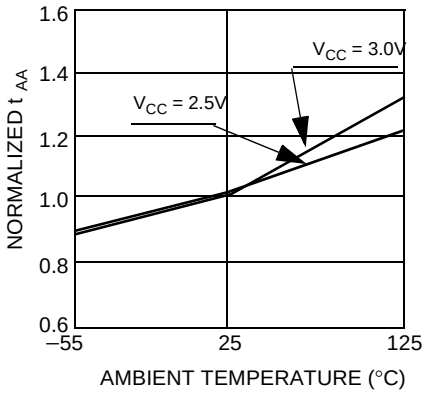
STANDBY CURRENT vs. AMBIENT TEMPERATURE



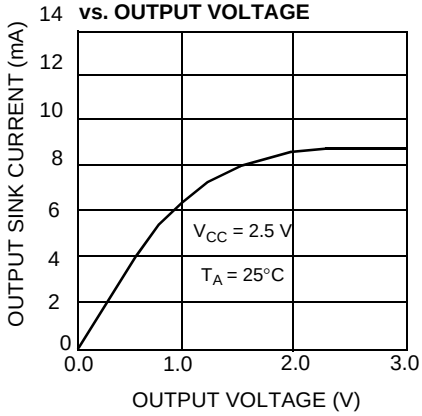
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



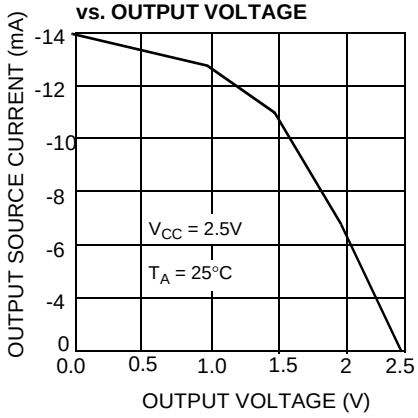
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

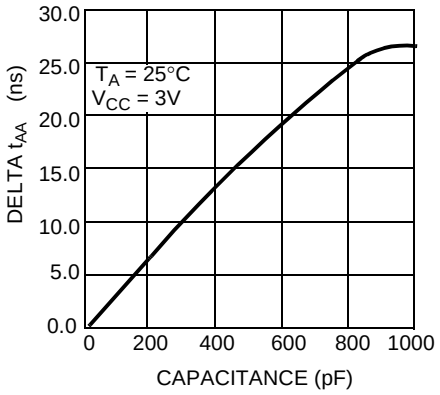


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

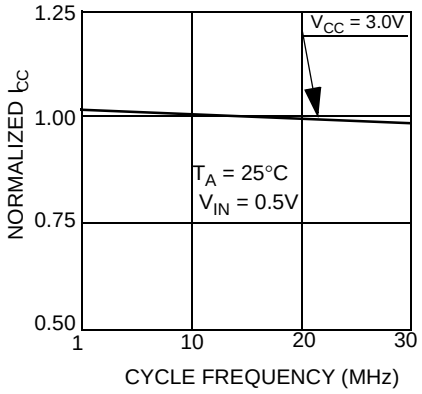


Typical DC and AC Characteristics (continued)

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs.CYCLE TIME



Truth Table

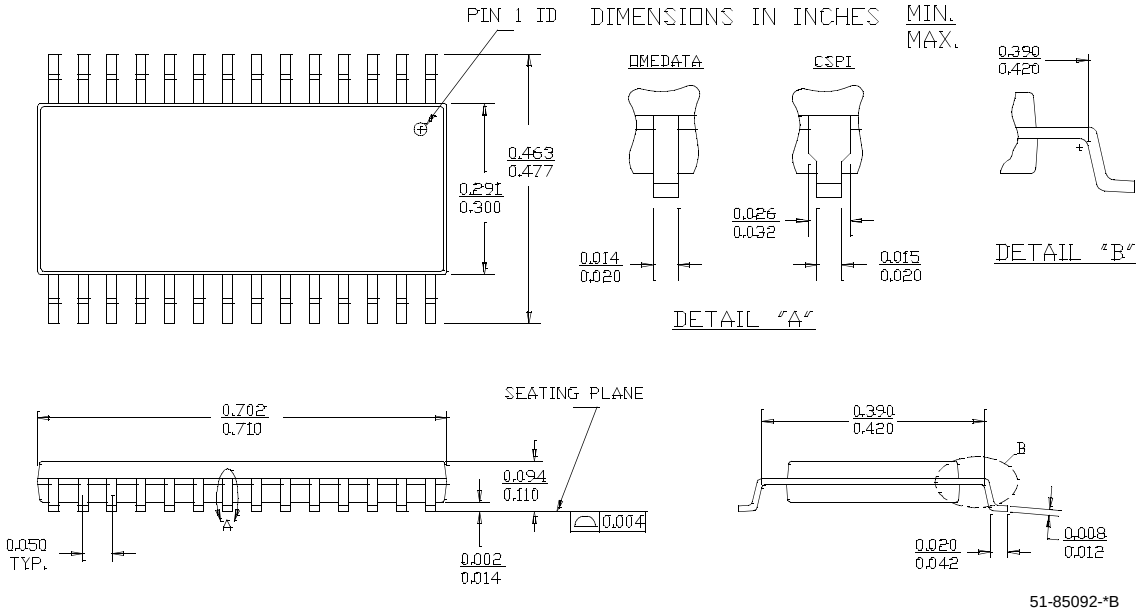
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62256VLL-70SNC	SN28	28-lead (300-mil Narrow Body) SOIC	Commercial
	CY62256VLL-70ZC	Z28	28-lead Thin Small Outline Package	Commercial
	CY62256VLL-70ZI			Industrial
	CY62256VLL -70SNI	SN28	28-lead (300-mil Narrow Body) SOIC	Industrial
	CY62256VLL-70ZRI	ZR28	28-lead Reverse Thin Small Outline Package	
100	CY62256V25LL-100ZC	Z28	28-lead Thin Small Outline Package	Commercial

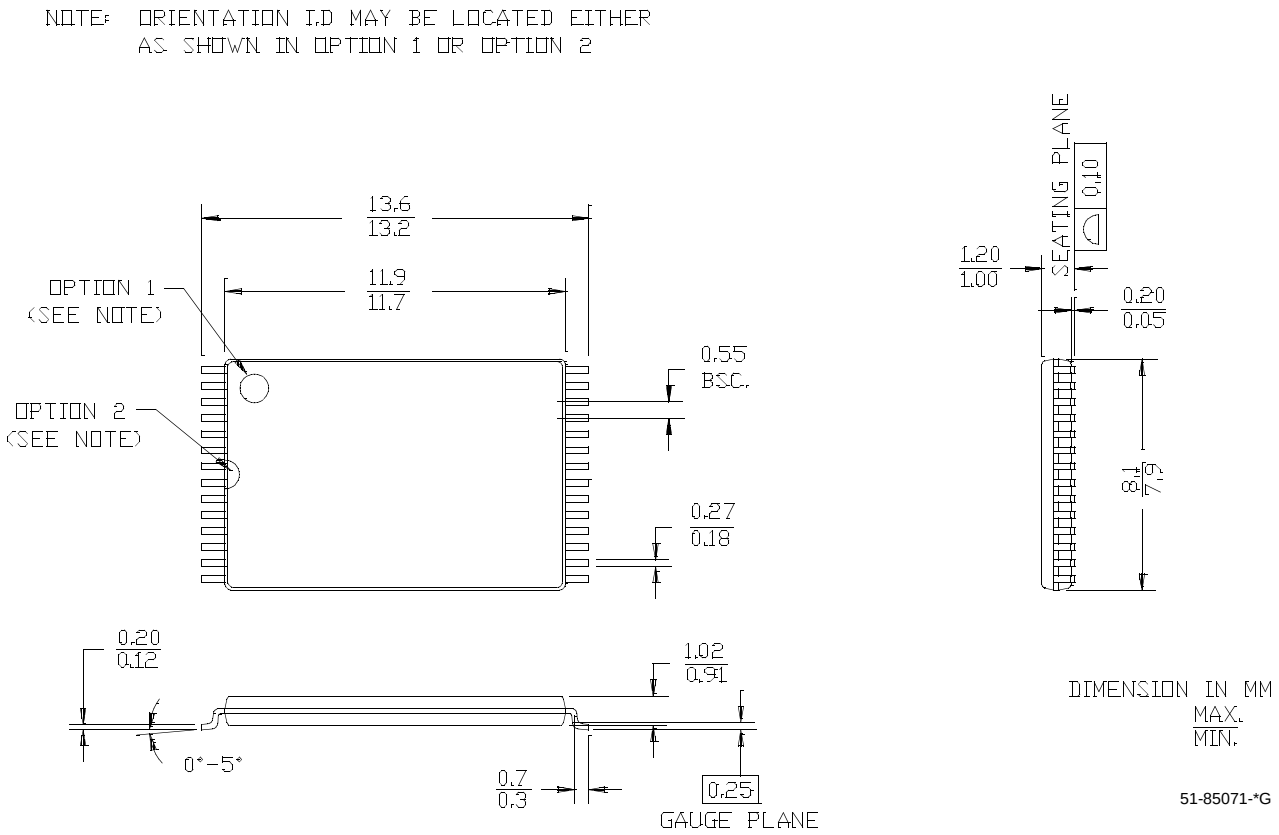
Package Diagrams

28-lead (300-mil) SNC (Narrow Body) SN28



51-85092-*B

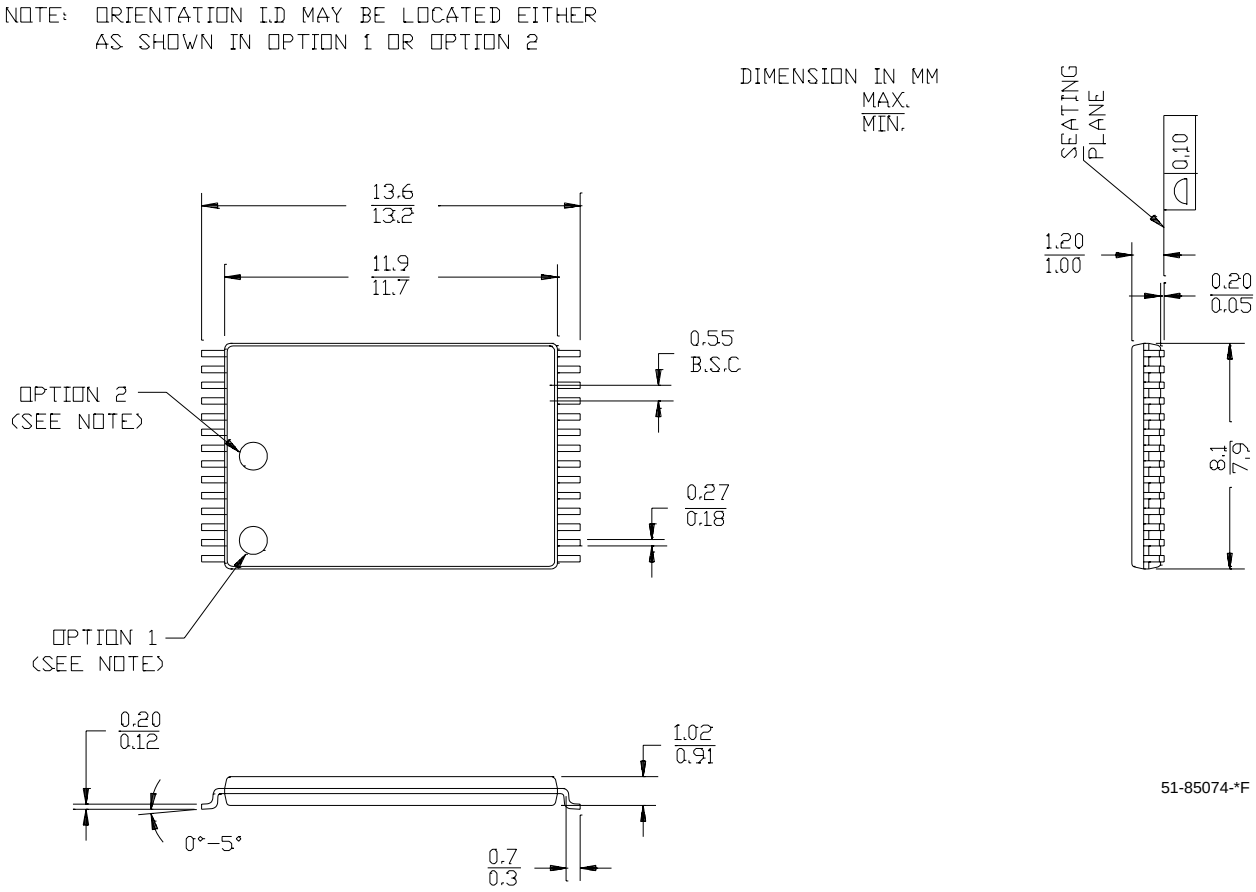
28-lead Thin Small Outline Package Type 1 (8 × 13.4 mm) Z28



51-85071-*G

Package Diagrams (continued)

28-lead Reverse Type 1 Thin Small Outline Package (8 × 13.4 mm) ZR28



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Document Title: CY62256V 32K x 8 Static RAM Document Number: 38-05057				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107248	09/10/01	SZV	Change from Spec number: 38-00519 to 38-05057.
*A	111445	11/01/01	MGN	Remove obsolete parts. Change to standard format.
*B	115229	05/23/02	GBI	Changed SN package diagram.